

Abstract of the Disclosure

10/00/557

Disclosed is a self-aligned non-volatile memory cell comprising a small sidewall spacer electrically coupled and being located next to a main floating gate region. Both the small sidewall spacer and the main floating gate region are formed on a substrate and both form the floating gate of the non-volatile memory cell. Both are isolated electrically from the substrate by an oxide layer which is thinner between the small sidewall spacer and the substrate; and is thicker between the main floating gate region and the substrate. The small sidewall spacer can be made small; therefore, the thin oxide layer area can also be made small to create a small pathway for electrons to tunnel into the floating gate.

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